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IN THE CLAIMS:

Please substitute the following amended claims for their corresponding claims:

1. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry, wherein the slurry modifier combined with CMP slurry polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate without the use of a dummy structure; and

polishing the silicon dioxide layer without polishing any dummy structure using the modifier-containing slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using any dummy structure.

5. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding a slurry modifier to the slurry, wherein the slurry modifier combines with the CMP slurry to enable polishing of low structure areas at a substantially zero rate and polishing of high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide layer without any dummy structures using the modifier-contained slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using a dummy structure.

8. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding ethylene glycol at a concentration of up to 50% for polishing low structure areas at a substantially zero rate and polishing high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide layer without any dummy structure using the slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using a dummy structure.

10. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer, and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry to produce a modified slurry that polishes the low structure areas at a substantially zero rate and polishes the high structure areas at a rate approximating a blanket polishing rate without relying on any dummy structure; and

polishing the silicon dioxide having high structure areas and low structure areas using the modified slurry, whereby high structure areas are polished at a rate approximating a blanket polishing rate and low structure areas are polished at a substantially zero rate.

13 (Thrice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas, without any dummy structure;

forming a CMP slurry having a high structure polishing rate lower than a blanket polishing rate;

adding a slurry modifier to the slurry to produce a modified slurry that polishes high structures at a rate approximating the blanket polishing rate; and

polishing the high structure areas of silicon dioxide, whereby the high structure areas are polished at a rate approximating the blanket polishing rate without using any dummy structure.

16. (Twice Amended). A method of chemically-mechanically polishing a silicon dioxide layer having high structure areas and low structure areas overlying a semiconductor substrate comprising:

forming a slurry comprising cerium oxide and ethylene glycol; and

polishing the silicon dioxide layer, without any dummy structure, such that the high structure areas are polished at a rate approximating a blanket polishing rate, and the low structure areas are polished at a substantially zero rate, without using any dummy structure.

17 (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas;

forming a CMP slurry having a low-density high structure polishing rate and a high-density high structure polishing rate, wherein the low-density high structure polishing rate is essentially the same as a high-density high structure polishing rate; and

polishing the high structure areas without the use of dummy structures, whereby the polishing rate is independent of pattern density.

Application Serial No. 09/270,606
Clean Set of Amended Claims

1. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry, wherein the slurry modifier combined with CMP slurry polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate without the use of a dummy structure; and

polishing the silicon dioxide layer without polishing any dummy structure using the modifier-containing slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using any dummy structure.

5. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding a slurry modifier to the slurry, wherein the slurry modifier combines with the CMP slurry to enable polishing of low structure areas at a substantially zero rate and polishing of high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide layer without any dummy structures using the modifier-contained slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using a dummy structure.

8. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer . and without any dummy structure;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding ethylene glycol at a concentration of up to 50% for polishing low structure areas at a substantially zero rate and polishing high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide layer without any dummy structure using the slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using a dummy structure.

10. (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer, and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry to produce a modified slurry that polishes the low structure areas at a substantially zero rate and polishes the high structure areas at a rate approximating a blanket polishing rate without relying on any dummy structure; and

polishing the silicon dioxide having high structure areas and low structure areas using the modified slurry, whereby high structure areas are polished at a rate approximating a blanket polishing rate and low structure areas are polished at a substantially zero rate.

13 (Thrice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas, without any dummy structure;

forming a CMP slurry having a high structure polishing rate lower than a blanket polishing rate;

adding a slurry modifier to the slurry to produce a modified slurry that polishes high structures at a rate approximating the blanket polishing rate; and

polishing the high structure areas of silicon dioxide, whereby the high structure areas are polished at a rate approximating the blanket polishing rate without using any dummy structure.

16. (Twice Amended). A method of chemically-mechanically polishing a silicon dioxide layer having high structure areas and low structure areas overlying a semiconductor substrate comprising:

forming a slurry comprising cerium oxide and ethylene glycol; and

polishing the silicon dioxide layer, without any dummy structure, such that the high structure areas are polished at a rate approximating a blanket polishing rate, and the low structure areas are polished at a substantially zero rate, without using any dummy structure.

17 (Twice Amended). A method of fabricating an integrated circuit using CMP comprising:

providing a substrate with an overlying silicon dioxide layer , and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas;

forming a CMP slurry having a low-density high structure polishing rate and a high-density high structure polishing rate, wherein the low-density high structure polishing rate is essentially the same as a high-density high structure polishing rate; and

polishing the high structure areas without the use of dummy structures, whereby the polishing rate is independent of pattern density.